# Ruibo Lu

CONTACT
INFORMATION

Jinhe Road, Dongxihu District
Wuhan, Hubei Province

reaperlu@hust.edu.cn
www.dingisoul.cn

EDUCATION

**Huazhong University of Science and Technology**, Wuhan, China          August 2022 -
M.E. in Network and Information Security, GPA: 87.7/100,
Advised by Dr. Wei Zhou

**Dalian University of Technology**, Dalian, China          June 2022
B.E. in Cyber Engineering, GPA: 88.6/100

PUBLICATIONS

Nino Nicolas*, **Ruibo Lu***, Wei Zhou, Kyu Hyung Lee, Ziming Zhao and Le Guan. "Unveiling IoT Security in Reality: A Firmware-Centric Journey." USENIX Security Symposium (2024). **\*equally contribution**

**Ruibo Lu**, Wei Zhou, Le Guan, Yuqing Zhang. "XXX" submitted to IEEE Symposium on Security and Privacy (2025)

Wei Zhou, **Ruibo Lu**. "Crash analysis method and device for Internet of Things Firmware." Chinese Patent 2024,103,089,256

HONORS AND
AWARDS

Merit Student Fellowship, Huazhong University of Science and Technology          2024
Panasonic Outstanding Student Fellowship, Dalian Unversity of Technology          2021
Academic Scholarship, HUST&DUT          2019-2024

PROJECTS

**FirmFlaw** Static Security Analysis of Large-Scale Real-World IoT Firmwares          [Code], [Web]
Code for USENIX Security 24
- **Function similarity** generation over millions of **binary** functions database
- **N-days vulnerability** detection based on similarity result
- Hardware mitigation detection based on static binary analysis

**XXX(Under-Review)** Low-Cost In-Field Crash Replay and Analysis for IoT Firmwares          [Code]

- High fidelity crash replay based on **symbolic execution** and **static analysis**
- Root cause analysis based on **symbolic execution**
- First author, **submit to IEEE S&P 25**

**QEMU-RVP/K** RISC-V Crypto Extension in QEMU          [Code]

- Implementation of crypto algorithms in QEMU
- **Merged by community**

WORKING
EXPERIENCE

**Institute of Software, Chinese Academy of Sciences**, remote          March 2022 - August 2023
Senior RISC-V Emulator Intern
- Leads the implementation of Xiangshan IP core's performance emulator
- Implementation of crypto instructions of RISC-V in QEMU
- Contributes to implementation of RISC-V Vector Extension in gem5

**Isyscore Intelligent Technology Co. Ltd.**, Hangzhou, China       November 2021 - Feburary 2022
Operating System Core Development Intern

- Responsible for containerizing backend code, decoupling dependencies
- developing the testing framework.

TEACHING
EXPERIENCE

**School of Software**, Dalian University of Technology, Dalian, Liaoning, China

*Teaching Assistant*                                           September - December 2021
Introduction to Artificial Intelligence

*Teaching Assistant*                                           September - December 2021
Advanced C language and network programming technology

SKILLS

- **Dynamic Analysis:** symbolic execution, dynamic taint analysis, address sanitizer etc.
- **Static Analysis:** control flow and data flow analysis based on Ghidra(expert)
- **Languages:** C / C++ (most commonly used), Python, Java, Rust